AMENDMENTS TO THE CLAIMS

1. (Currently amended) An apparatus for generating a channelization code, comprising:

a binary counter circuit that is arranged to: receive a spreading factor signal and a clock signal, provide a binary count signal that is responsive to the clock signal, and reset the binary counter circuit when the binary count signal reaches a limit number that is associated with a spreading factor, wherein the spreading factor is associated with the spreading factor signal;

a code logic circuit that is arranged to: receive a code number signal and the spreading factor signal, and provide a right-justified code signal in response to the code number signal and the spreading factor signal, wherein the right-justified code signal corresponds to a right justified version of the code number signal;

a register circuit that is arranged to: receive the right-justified code signal and the clock signal, store the right-justified code signal in response to the clock signal, and provide the stored right-justified code signal as a stored code signal; and

a channelization logic circuit that is arranged to: receive the stored code signal and the binary count signal, and provide the channelization code in response to the stored code signal and the binary count signal such that the channelization code is associated with the code number and the spreading factor.

2. (Currently amended) An apparatus for generating a channelization code, comprising:

a binary counter circuit that is arranged to: receive a spreading factor signal and a clock signal, provide a binary count signal that is responsive to the clock signal, and reset the binary counter circuit when the binary count signal reaches a limit number that is associated with a spreading factor, wherein the spreading factor is associated with the spreading factor signal~~The apparatus of Claim 1~~, wherein the limit number is equal to the spreading factor minus one;

a code logic circuit that is arranged to: receive a code number signal and the spreading factor signal, and provide a right-justified code signal in response to the code number signal and the spreading factor signal, wherein the right-justified code signal corresponds to a right justified version of the code number signal;

a register circuit that is arranged to: receive the right-justified code signal and the clock signal, store the right-justified code signal in response to the clock signal, and provide the stored right-justified code signal as a stored code signal; and

a channelization logic circuit that is arranged to: receive the stored code signal and the binary count signal, and provide the channelization code in response to the stored code signal and the binary count signal such that the channelization code is associated with the code number and the spreading factor.

3. (Original) The apparatus of Claim 1, wherein the register circuit comprises a plurality of flip-flops, and wherein each of the plurality of flip-flops is configured to store one bit of the right-justified code number signal.

4. (Original) The apparatus of Claim 1, wherein the binary counter circuit comprises a binary counter and a digital comparator, an output of the digital comparator is coupled to a reset input of the binary counter, and wherein the digital comparator is configured to compare the binary count to the limit number.

5. (Original) The apparatus of Claim 1, wherein the binary counter circuit comprises a binary counter, a digital comparator, and an OR gate, the OR gate has a first OR input, a second OR input, and an OR output, the digital comparator has a comparator output, the digital comparator is configured to compare the binary count to the limit number, the comparator output is coupled to the first OR input, the OR gate is configured to receive a frame reset signal at the second OR input, the frame reset signal is active when at least one of the code number or the spreading factor changes, and wherein the OR output is coupled to a reset input of the binary counter, such that the binary counter is reset when the frame reset signal is active or the binary count reaches the limit number.

6. (Original) The apparatus of Claim 1, wherein the binary counter circuit has a counter output, the binary counter circuit is configured to provide the binary count signal at the counter output, the counter output has a number of bits that is equal to a first number, the register circuit has a register output, the register circuit is configured to provide the stored code number at the register output, and wherein the register output has a number of bits that is equal to the first number.

7. (Original) The apparatus of Claim 6, wherein the channelization logic circuit comprises a number of logic gates that is approximately equal to twice the first number.

8. (Original) The apparatus of Claim 6, wherein the channelization logic circuit comprises a plurality of AND gate circuits, the channelization logic circuit further comprises a plurality of XOR gate circuits, the number of the plurality of AND gate circuits corresponds to the first number, and the number of the plurality of XOR gate circuits corresponds to the first number.

9. (Original) The apparatus of Claim 8, wherein each of the plurality of AND gate circuits has a first input, a second input, and an output, each of the plurality of AND gate circuits is configured to provide an AND output signal at the output of the AND gate circuit in response to a signal that is provided at the first input of the AND gate circuit and the second input of the AND gate circuit, each of the plurality of XOR gate circuits has a first input, a second input, and an output, each of the plurality of XOR gate circuits is configured to provide an XOR output signal at the output of the XOR gate circuit in response to a signal that is provided at the first input of the XOR gate circuit and the second input of the XOR gate circuit, the output of each AND gate circuit is coupled to first input of a corresponding XOR gate circuit, the first XOR gate circuit is configured to provide the channelization code at the output of the first XOR gate circuit, the output of each of the XOR gate circuits other than the first XOR gate circuit is coupled to the second input of the previous XOR gate circuit, the first input of the first of the plurality of AND gate circuits is coupled to a least significant bit of the counter output, the second input of the first of the plurality of AND gate circuits is coupled to a most significant bit of the register output, the first input of each subsequent AND gate circuit of the plurality of AND gate circuits is coupled to a next least significant bit of the counter output, and the second input of each subsequent AND gate circuit of the plurality of AND gate circuits is coupled to a next most significant bit of the register output.

10. (Original) The apparatus of Claim 6, wherein the first number is eight such that the counter output comprises a counter bit 0, a counter bit 1, a counter bit 2, a counter bit 3, a counter bit 4, a counter bit 5, a counter bit 6, and a counter bit 7 such that the counter bit 7 is the most significant bit and the counter bit 0 is the least significant bit of the counter output, and wherein the register output comprises a register bit 0, a register bit 1, a register bit 2, a register bit 3, a register

bit 4, a register bit 5, a register bit 6, and a register bit 7 such that the register bit 7 is the most significant bit and the register bit 0 is the least significant bit of the register output.

11. (Original) The apparatus of Claim 10, wherein the channelization logic circuit comprises:

a first AND gate having a first input, a second input, and a first output, wherein the first input is coupled to the counter bit 7 and the second input is coupled to the register bit 0;

a second AND gate having a third input, a fourth input, and a second output, wherein the third input is coupled to the counter bit 6 and the fourth input is coupled to the register bit 1;

a third AND gate having a fifth input, a sixth input, and a third output, wherein the fifth input is coupled to the counter bit 5 and the sixth input is coupled to the register bit 2;

a fourth AND gate having a seventh input, a eighth input, and a fourth output, wherein the seventh input is coupled to the counter bit 4 and the eighth input is coupled to the register bit 3;

a fifth AND gate having a ninth input, a tenth input, and a fifth output, wherein the ninth input is coupled to the counter bit 3 and the tenth input is coupled to the register bit 4;

a sixth AND gate having a eleventh input, a twelfth input, and a sixth output, wherein the eleventh input is coupled to the counter bit 2 and the twelfth input is coupled to the register bit 5;

a seventh AND gate having a thirteenth input, a fourteenth input, and a seventh output, wherein the thirteenth input is coupled to the counter bit 1 and the fourteenth input is coupled to the register bit 6;

a eighth AND gate having a fifteenth input, a sixteenth input, and a eighth output, wherein the fifteenth input is coupled to the counter bit 0 and the sixteenth input is coupled to the register bit 7;

a first XOR gate having a seventeenth input, an eighteenth input, and a first XOR output, wherein the seventeenth input is configured to receive a signal having a voltage that corresponds to a logical level of zero, and the eighteenth input is coupled to the first output;

a second XOR gate having a nineteenth input, a twentieth input, and a second XOR output, wherein the nineteenth input is coupled to the first XOR output, and the twentieth input is coupled to the second output;

a third XOR gate having a twenty-first input, a twenty-second input, and a third XOR output, wherein the twenty-first input is coupled to the second XOR output, and the twenty-second input is coupled to the third output;

a fourth XOR gate having a twenty-third input, a twenty-fourth input, and a fourth XOR output, wherein the twenty-third input is coupled to the third XOR output, and the twenty-fourth input is coupled to the fourth output;

a fifth XOR gate having a twenty-fifth input, a twenty-sixth input, and a fifth XOR output, wherein the twenty-fifth input is coupled to the fourth XOR output, and the twenty-sixth input is coupled to the fifth output;

a sixth XOR gate having a twenty-seventh input, a twenty-eighth input, and a sixth XOR output, wherein the twenty-seventh input is coupled to the fifth XOR output, and the twenty-eighth input is coupled to the sixth output;

a seventh XOR gate having a twenty-ninth input, a thirtieth input, and a seventh XOR output, wherein the twenty-ninth input is coupled to the sixth XOR output, and the thirtieth input is coupled to the seventh output;

a eighth XOR gate having a thirty-first input, a thirty-second input, and a eighth XOR output, wherein the thirty-first input is coupled to the seventh XOR output, the thirty-second input is coupled to the eighth output, and wherein the eighth XOR output corresponds to the channelization code output.

12. (Currently amended) A method for producing a channelization code in response to a spreading factor and a code number, the method comprising:

comparing a binary count to a limit number;

incrementing the binary count in response to a clock signal when the binary count is less than the limit number;

resetting the binary count when the binary count is equal to the limit number, wherein the limit number is related to the spreading factor;

evaluating a code number and the spreading factor;

right justifying the code number based on the spreading factor;

storing the right-justified code number as a stored code number; and

logically calculating the channelization code in response to the binary count and the stored code number.

13. (Currently amended) A method for producing a channelization code in response to a spreading factor and a code number, the method comprising:

comparing a binary count to a limit number;

incrementing the binary count in response to a clock signal when the binary count is less than the limit number;

resetting the binary count when the binary count is equal to the limit number, wherein the limit number is related to the spreading factor;

evaluating a code number and the spreading factor~~The method as in Claim 12~~, wherein the limit number is equal to the spreading factor minus one;

evaluating a code number and the spreading factor;

right justifying the code number based on the spreading factor;

storing the right-justified code number as a stored code number; and

logically calculating the channelization code in response to the binary count and the stored code number.

14. (Original) The method of Claim 12, wherein right-justifying the code number comprises:

determining a number of valid bits of the code number, wherein the number of valid bits of the code number corresponds to the base two logarithm of the spreading factor, and wherein the code number is a binary number;

setting the most significant bit of the right-justified code number to the most significant valid bit of the code number;

for each remaining valid bit of the code number, setting the next most significant bit of the right-justified code number to the next most significant valid bit of the code number; and

setting the remaining bits of the right-justified code number to zero.

15. (Original) The method of Claim 12, wherein the binary count comprises a number of bits that is equal to a first number, the stored code number comprises a number of bits that is equal to the first number, and wherein logically calculating the channelization code comprises:

providing a first of a plurality of AND signals, wherein the first of the plurality of AND signals is provided such that the first of the plurality of AND signals corresponds to a logical level of one when a first condition is satisfied and the first of the plurality of bits corresponds to a logical level of zero when the first condition is not satisfied, and wherein the first condition is satisfied when a most significant bit of the binary count and the least significant bit of the stored code number both correspond to zero;

providing each subsequent AND signal of the plurality of AND signals, wherein each subsequent AND signal of the plurality of AND signals is provided such that the next of the plurality of AND signals corresponds to a logical level of one when a next condition is satisfied and the next of the plurality of bits corresponds to a logical level of zero when the next condition is not satisfied, and wherein the next condition is satisfied when a next most significant bit of the binary count and the next least significant bit of the stored code number both correspond to zero;

providing a first of a plurality of XOR signals, wherein the first of the plurality of XOR signals is provided such that the first of the plurality of XOR signals corresponds to a logical level of one when a first XOR condition is satisfied and the first of the plurality of bits corresponds to a logical level of zero when the first XOR condition is not satisfied, and wherein the first XOR condition is satisfied when the first of the plurality of AND signals corresponds to a logical level of one;

providing a next of the plurality of XOR signals, wherein the next of the plurality of XOR signals is provided such that the next of the plurality of XOR signals corresponds to a logical level of one when a next XOR condition is satisfied and the next of the plurality of bits corresponds to a logical level of zero when the next XOR condition is not satisfied, the next XOR condition is satisfied when the next of the plurality of AND signals and the previous XOR signal each correspond to different logical levels, and wherein the last of the plurality of XOR signals corresponds to the channelization code.

16. (Original) An apparatus for generating a channelization code in response to a spreading factor and a code number, the apparatus comprising:

a means for counting that is configured to provide a binary count;

a means for resetting that is configured to reset the binary count when the binary count signal reaches a limit number, wherein the limit number corresponds to the spreading factor minus one;

a means for right justifying, wherein the means for right justifying is configured to right justify the code number in response to the spreading factor to provide a right-justified code number;

a means for storing, wherein the means for storing is configured to store the right-justified code number as a stored code number; and

a means for logically calculating that is configured to logically calculate the channelization code in response to the binary count and the stored code number.

17. (Currently amended) An apparatus for generating a channelization code in response to a spreading factor and a code number, the apparatus comprising:

a means for counting that is configured to provide a binary count;

a means for resetting that is configured to reset the binary count when the binary count signal reaches a limit number, wherein the limit number corresponds to the spreading factor minus one~~The apparatus of Claim 16~~, wherein the binary count comprises a number of bits that is equal to a first number, and wherein the stored code number has a number of bits that is equal to the first number;

a means for right justifying, wherein the means for right justifying is configured to right justify the code number in response to the spreading factor to provide a right-justified code number;

a means for storing, wherein the means for storing is configured to store the right-justified code number as a stored code number; and

a means for logically calculating that is configured to logically calculate the channelization code in response to the binary count and the stored code number.

18. (Original) The apparatus of Claim 17, wherein the means for logically calculating comprises logic gates, and wherein the number of logic gates is approximately equal to a second number, wherein the second number is twice the first number.

19. (Original) The apparatus of Claim 17, wherein the means for logically calculating comprises a plurality of means for providing an AND function, the means for logically calculating further comprises a plurality of means for providing an XOR function, the number of the plurality of means for providing an AND function corresponds to the first number, and the number of the plurality of means for providing an XOR function corresponds to the first number.

20. (Original) The apparatus of Claim 19, wherein each of the plurality of means for providing an AND function has a first input, a second input, and an output, each of the plurality of means for providing an AND function is configured to provide an AND output signal at the output of the means for providing an AND function in response to a signal that is provided at the first input of the means for providing an AND function and the second input of the means for providing an AND function, each of the plurality of means for providing an XOR function has a first input, a second input, and an output, each of the plurality of means for providing an XOR function is configured to provide an XOR output signal at the output of the means for providing an XOR function in response to a signal that is provided at the first input of the means for providing an XOR function and the second input of the means for providing an XOR function, the output of each means for providing an AND function is coupled to first input of a corresponds means for providing an XOR function, the first means for providing an XOR function is configured to provide the channelization code at the output of the first means for providing an XOR function, the output of each of the means for providing an XOR function other than the first means for providing an XOR function is coupled to the second input of the previous means for providing an XOR function, the first input of the first of the plurality of means for providing an AND function is configured to receive to a least significant bit of the binary count, the second input of the first of the plurality of means for providing an AND function is configured to receive a most significant bit of the stored code number, the first input of each subsequent means for providing an AND function of the plurality of means for providing an AND function is configured to receive a next least significant bit of the binary count, and the second input of each subsequent means for providing an AND function

of the plurality of means for providing an AND function is configured to receive a next most significant bit of the stored code number.